Drawing Package Supplement to WARLORDS™

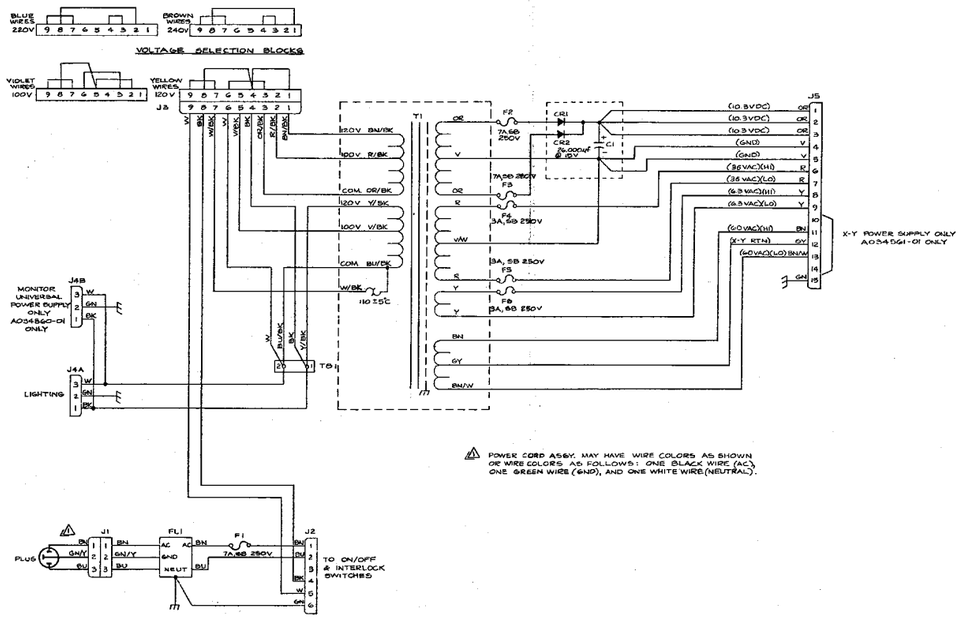
Operation, Maintenance and Service Manual

Contents of this Drawing Package

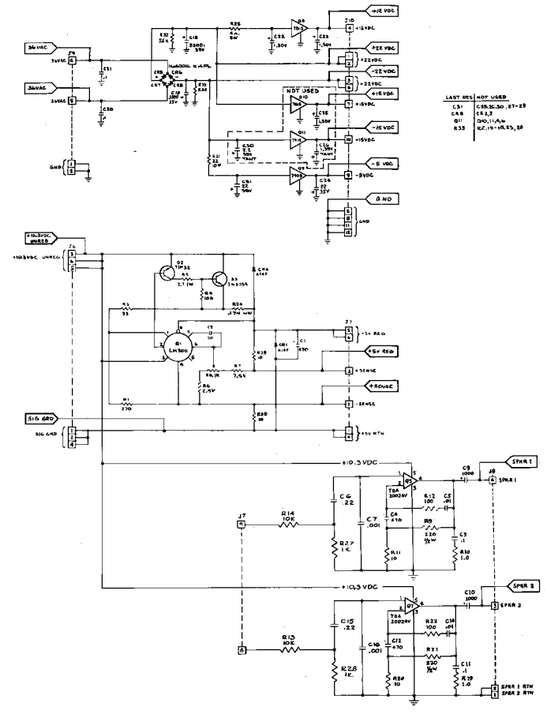
A Warner Communications Company

Sheet 1, Side A
DP-175-01 1st printing

X-Y Video Power Supply Wiring Diagram (034633-01 B)



Regulator Audio II PCB Schematic (035435-02 C)



Regulator/Audio II PCB

The Regulator/Audio II PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high-impedance inputs +SENSE and −SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

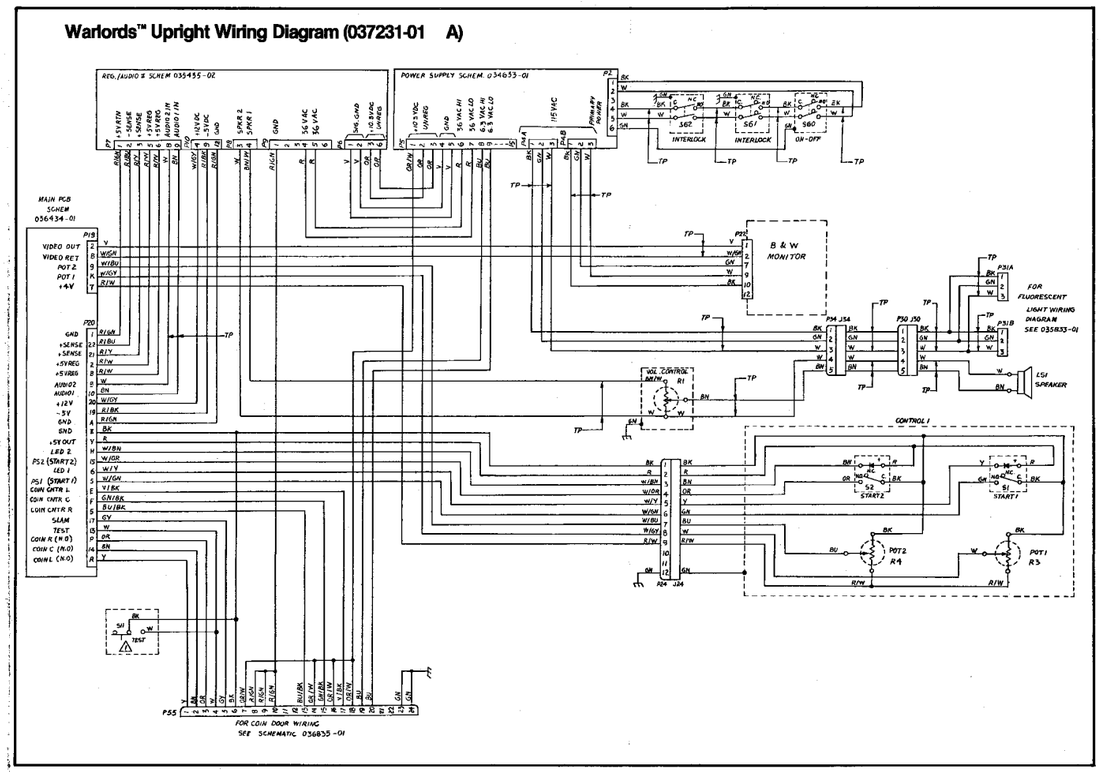
Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio II PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio II PCB. Voltage reading must not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio II PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio II PCB and plus lead to GND test point of game PCB. Note the voltage.
   Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio II PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

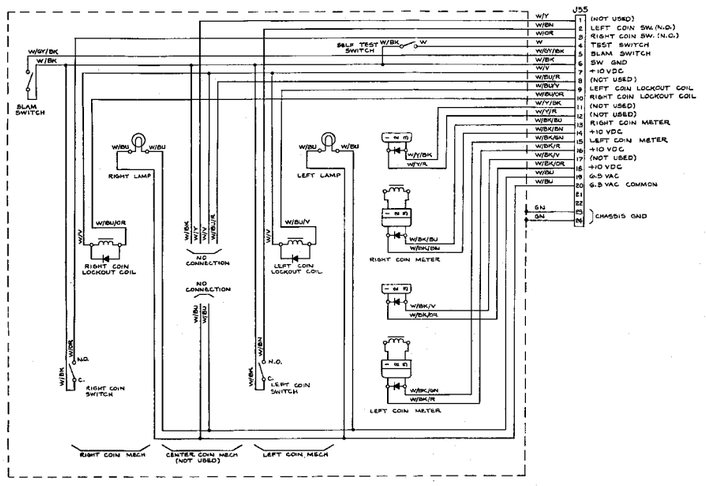
Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten.

Warlords™ Upright Wiring Diagram (037231-01 A)



Double Mech Coin Door Wiring Diagram (036835-01 A)



ATARI®

Sheet 1, Side B

WARLORDS™

Sync Generator
MPU
Address Decoder
RAM
ROM
Power Input

Section of 036434-01 B

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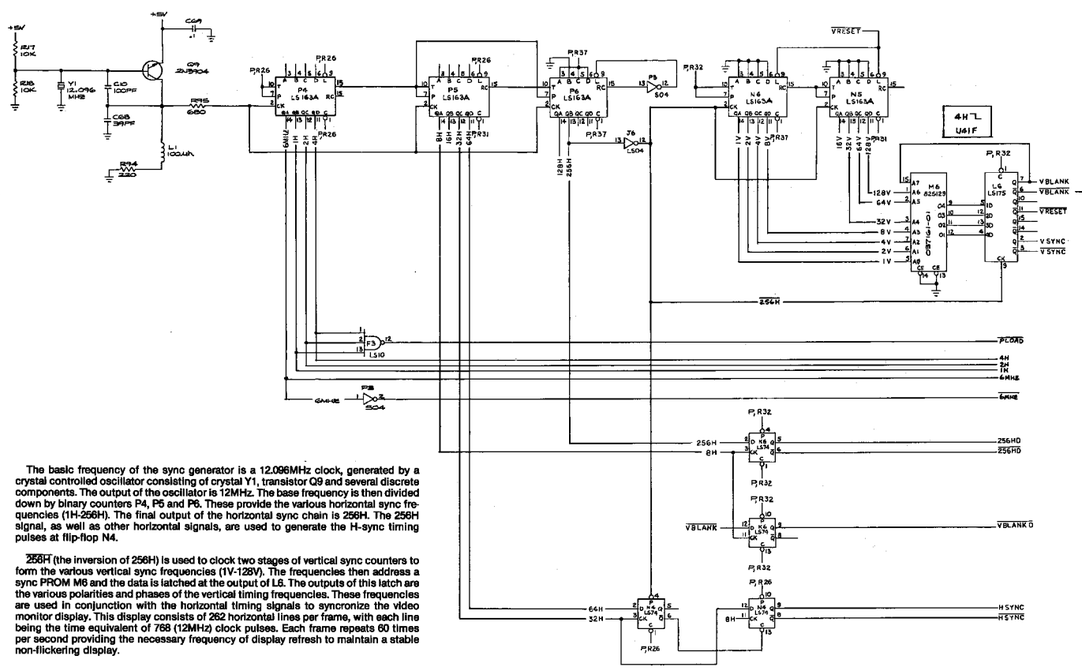
Sync Generator Circuitry

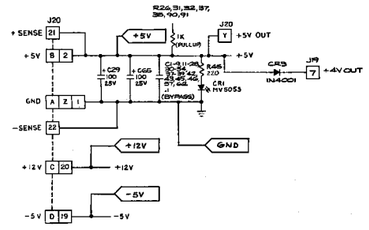


The basic frequency of the sync generator is a 12.096MHz clock, generated by a crystal controlled oscillator consisting of crystal Y1, transistor Q9 and several discrete components. The output of the oscillator is 12MHz. The base frequency is then divided down by binary counters P4, P5 and P6. These provide the various horizontal sync frequencies (1H-256H). The final output of the horizontal sync chain is 256H. The 256H signal, as well as other horizontal signals, are used to generate the H-sync timing pulses at flip-flop N4.

256H (the inversion of 256H) is used to clock two stages of vertical sync counters to form the various vertical sync frequencies (1V-128V). The frequencies then address a sync PROM M6 and the data is latched at the output of L6. The outputs of this latch are the various polarities and phases of the vertical timing frequencies. These frequencies are used in conjunction with the horizontal timing signals to syncronize the video monitor display. This display consists of 262 horizontal lines per frame, with each line being the time equivalent of 768 (12MHz) clock pulses. Each frame repeats 60 times per second providing the necessary frequency of display refresh to maintain a stable non-flickering display.

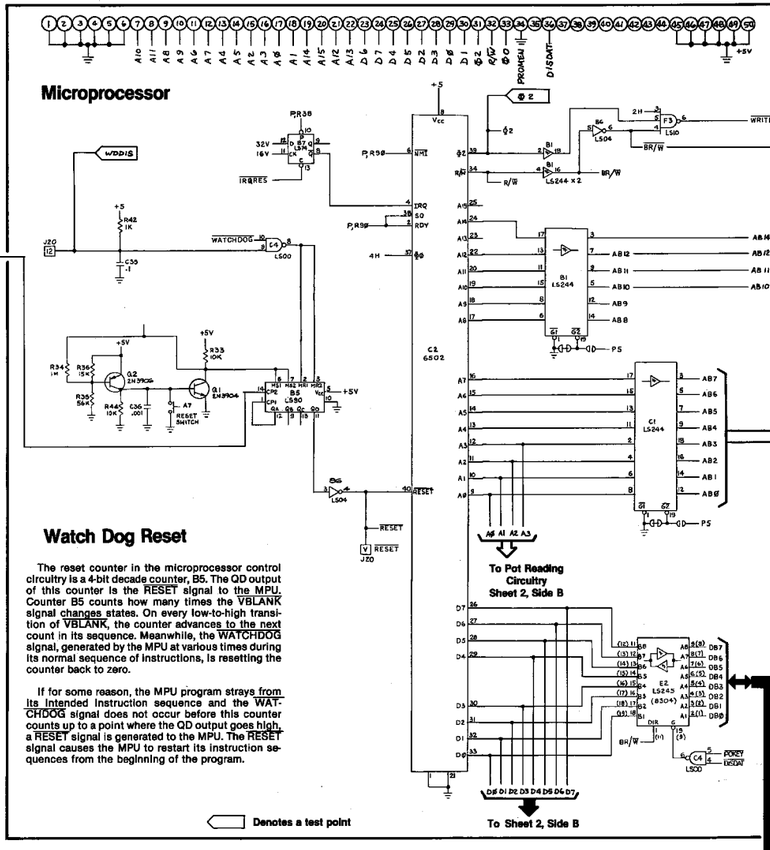
Denotes a signature

Power Input Circuitry



Denotes a test point

Microprocessor



Denotes a test point

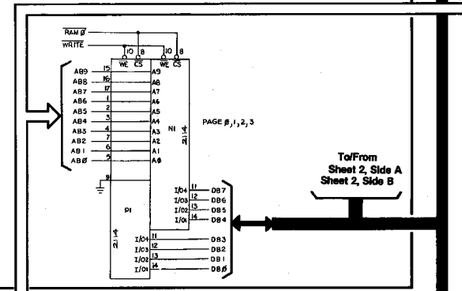
Watch Dog Reset

The reset counter in the microprocessor control circuitry is a 4-bit decade counter, B5. The QD output of this counter is the RESET signal to the MPU. Counter B5 counts how many times the VBLANK signal changes states. On every low-to-high transition of VBLANK, the counter advances to the next count in its sequence. Meanwhile, the WATCHDOG signal, generated by the MPU at various times during its normal sequence of instructions, is resetting the counter back to zero.

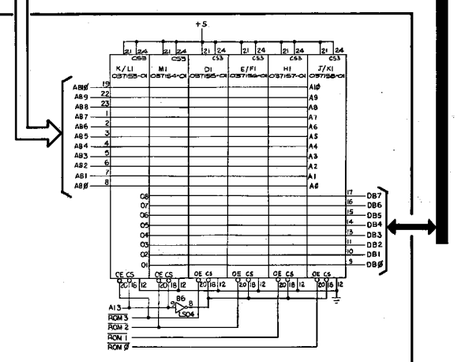
If for some reason, the MPU program strays from its intended instruction sequence and the WATCHDOG signal does not occur before this counter counts up to a point where the QD output goes high, a RESET signal is generated to the MPU. The RESET signal causes the MPU to restart its instruction sequences from the beginning of the program.

RAM Circuitry

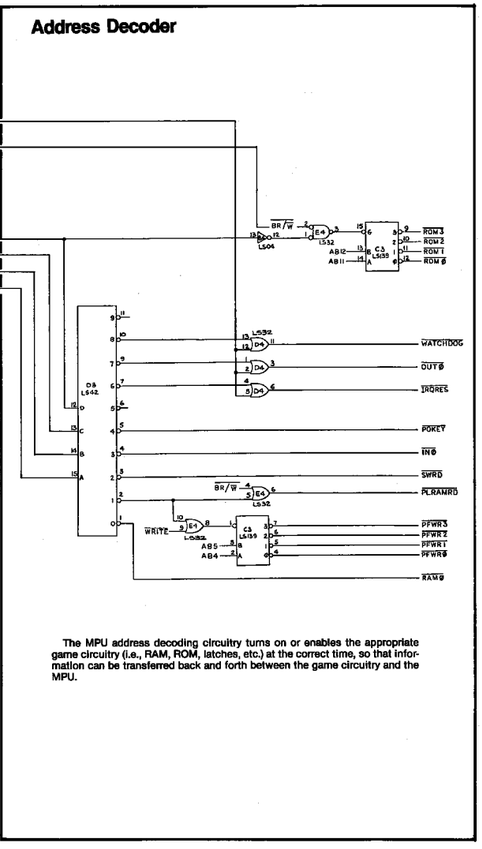
The MPU uses RAM memory to temporarily store information which it will later recall. The MPU is capable of writing (putting data into) the RAM and then later reading (pulling data out of) the RAM, via address bus A80-A89 and bidirectional data bus DB0-DB7.



ROM Circuitry



Address Decoder



The MPU address decoding circuitry turns on or enables the appropriate game circuitry (i.e., RAM, ROM, latches, etc.) at the correct time, so that information can be transfered back and forth between the game circuitry and the MPU.

MEMORY MAP

HEXA-DECIMAL ADDRESS	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		D	D	D	D	D	D	D	D	Program RAM
0400-07BF		D	D	D	D	D	D	D	D	Playfield RAM
07C0-07DF		D	D	D	D	D	D	D	D	Picture Code
07D0-07DF		D	D	D	D	D	D	D	D	Vert. Position
07E0-07EF		D	D	D	D	D	D	D	D	Horiz. Position
0800	R			D						1 Player Cost
	R				D					2-4 Player Cost
	R					D				High-Score Music
	R							D	D	Foreign Language
0801	R							D	D	No. of Coins Per Credit
	R					D	D			Right Coin Mech
	R				D					Left Coin Mech
	R	D	D	D						Bonus Coin Adder
0C00	R	D								Upright/Cocktail
	R		D							VBLANK
	R			D						Self-Test Switch
0C01	R	D								Left Coin Switch
	R		D							Center Coin Switch
	R			D						Right Coin Switch
	R				D					Slam Switch
	R					D				Player Start (PS4)
	R						D			Player Start (PS3)
	R							D		Player Start (PS2)
	R								D	Player Start (PS1)
1000-100F		D	D	D	D	D	D	D	D	Custom Audio Chip
1800										IRQ Reset
1C00	W	D								Right Coin Counter
1C01	W	D								Center Coin Counter
1C02	W	D								Left Coin Counter
1C03	W	D								LED 1
1C04	W	D								LED 2
1C05	W	D								LED 3
1C06	W	D								LED 4
4000	W									Watchdog
5000-7FFF	R	D	D	D	D	D	D	D	D	Program ROM